Tribology and Moore’s law, how friction and wear challenge Next generation of chip manufacturing

ASML tribology competence

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Introduction to ASML lithography machines

DUV

EUV

$$CD = k_1 \cdot \frac{\lambda}{NA}$$

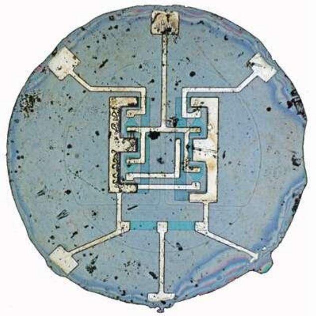
Moore law…

1940s
mm range transistor

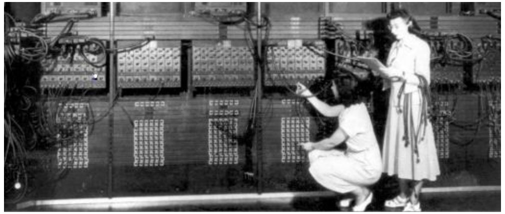
1980s
µm range transistor

2010
Tens of nm transistor

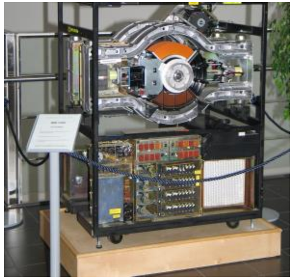
2020
5 to 7 nm transistors



First IC invented by Robert Noyce



ENIAC programmers



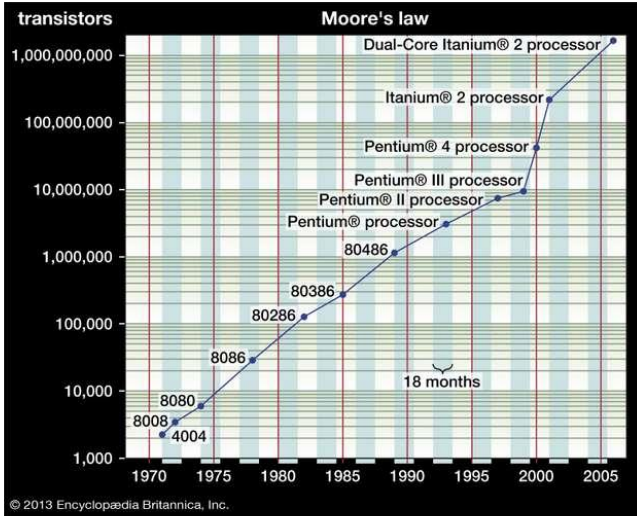
IBM 3380 first 1GB storage unit

Western Digital WD20EADS

6.9 billion transistors (7nm EUV) for both A12 (iphone) and Kiring 980 (Huawei)

11.8 billion transistors, A14 Iphone (5 nm EUV)

"Cramming more components onto integrated circuits", April 1965 Elect Electronic Magazine



"Smaller, faster and cheaper"

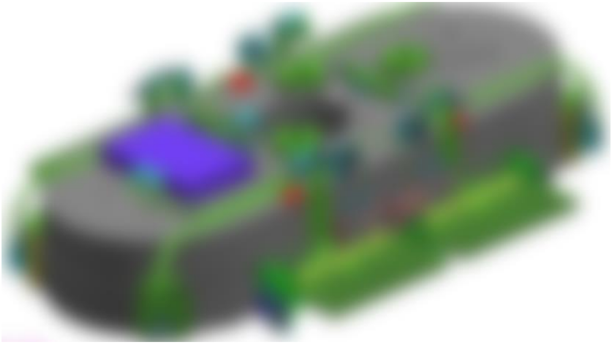
Not without challenges

Tribology across scales at ASML

ASML

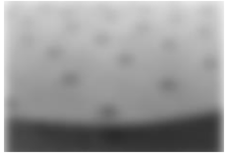
NXE 3300 TMSU*

NXE Reticle long stroke



Wafer handler

Wafer table



> 1 m

10^{-6} m

Tribology competence

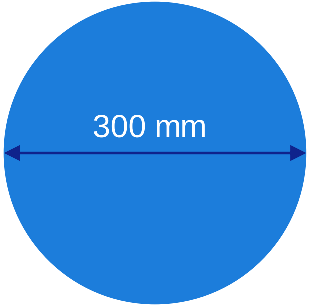
Maintain Tribology roadmap + Research ⟷ Identify knowledge gaps, new ideas, Feasibility ⟷ Collaborate with Research institutes ⟷ Formulate design rules ⟷ Support D&E

** TMSU: Top Module Service Unit*

Few examples of ASML wafer table micro/nanoscale challenges

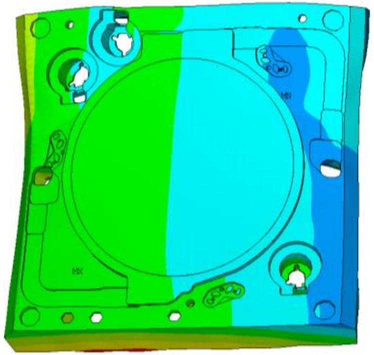
Wafer table flatness

1 nm



1 mm

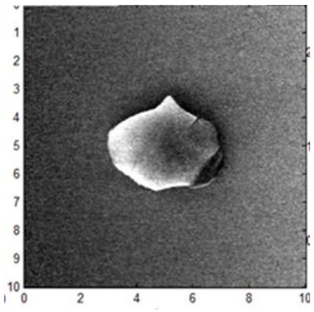
Wafer stage accelerations

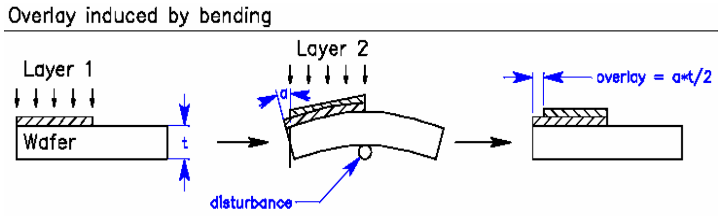


0 to 100km/h → 0.3 s

0 to 100 km/h → 2.4 s

Particle contamination





Contamination on wafer backside will induce overlay penalty of 0.5*α* t.

α: local angle

t: thickness of wafer

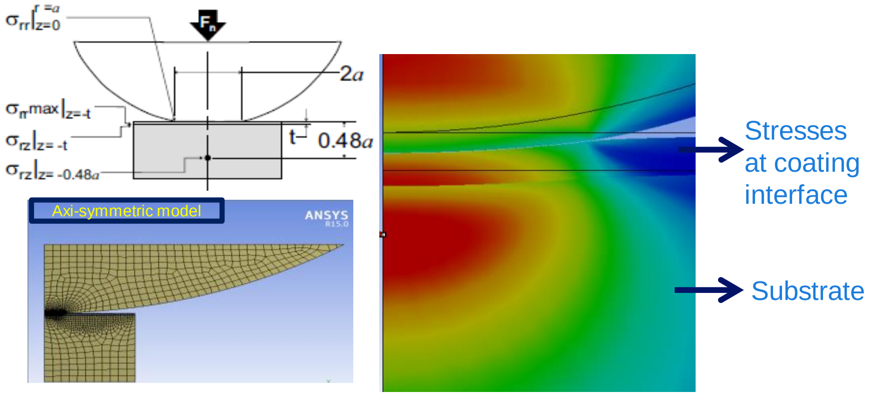
How does tribology competence contribute to address those challenges

Experiments

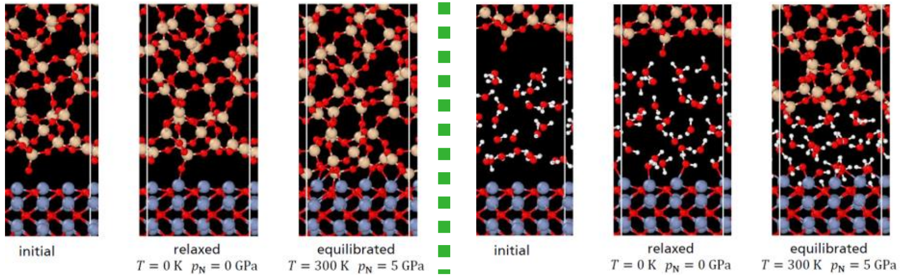
Various experimental setup operating in various load range and environmental conditions

Modeling

- ❑ Mechanical: Stress concentration on coated wafers



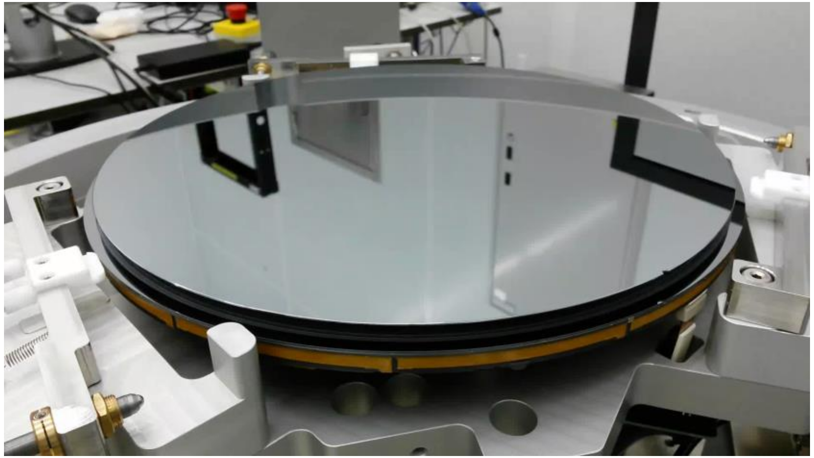
- ❑ Quantum chemistry + Molecular dynamics

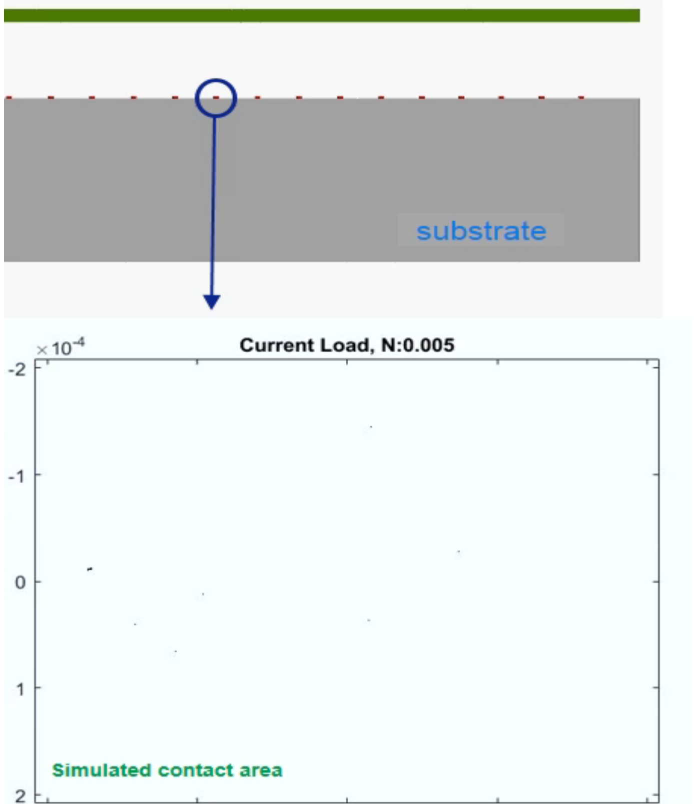


Simulation of contact between material A and B in vacuum and in presence of various chemical elements to understand fundamentals

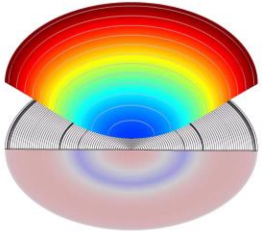
Tribology and contact mechanics in water tables

Wafer clamping onto wafer table DUV

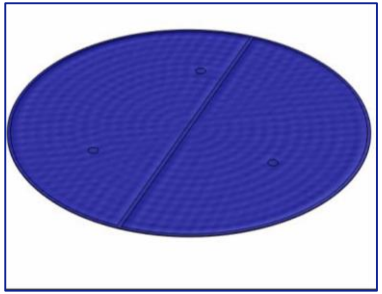




Wafer landing model DUV



Wafer unloading model EUV

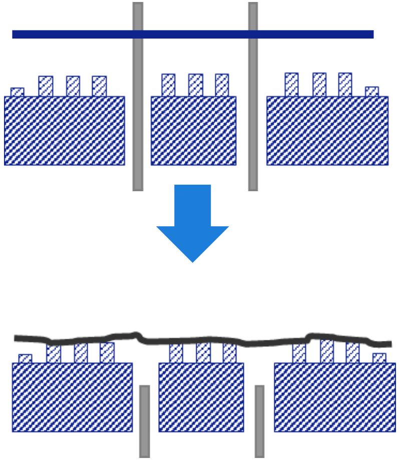


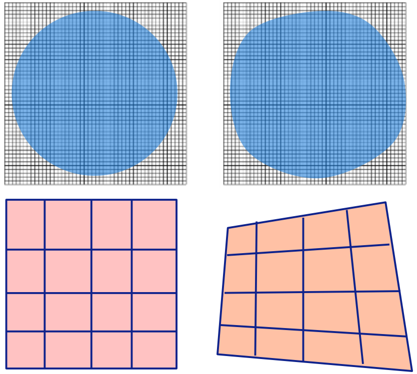
Wafer Load Grid (WLG), friction, interfacial shear strength

ASML

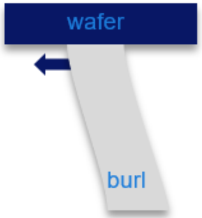
WLG

Stress in wafer induces combined with friction and wafer table interface induce grid deformation





Initial grid   Distorted grid

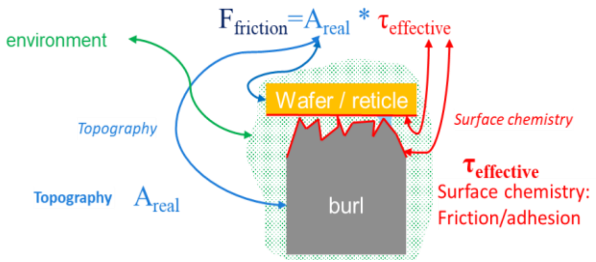


WLG α L*C*Ff

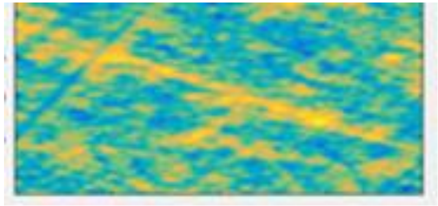
Loading parameters

- Wafer clamping force, rate etc…

Correction factors



Real contact area



Existing BEM based tool to simulate real contact area

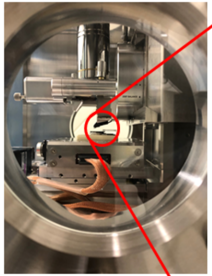
Shear strength

Assessing effective shear strengths (at time zero but also throughout lifetime of wafer tables) is a bit more in its early developments

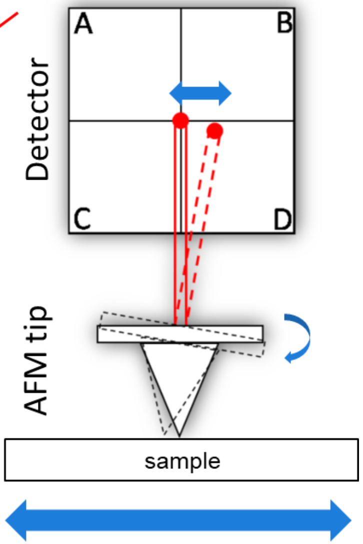
Multiscale approach to assess shear strength

LFM

NX-Hivac AFM



Side-view into the vacuum chamber of the AFM.

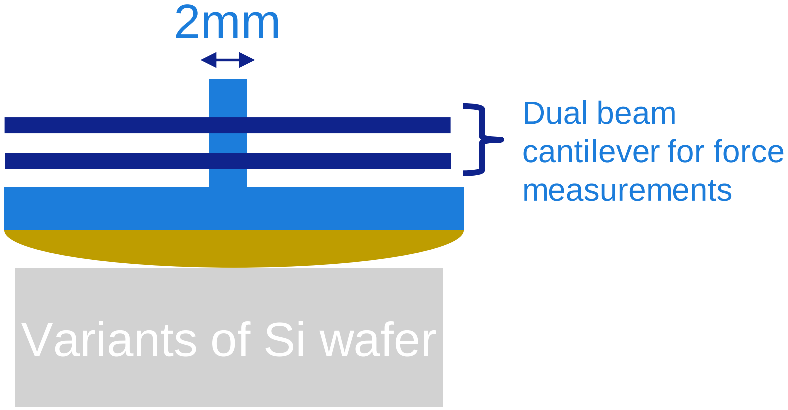


1. Lateral movement over the sample will induce a friction force between AFM tip and the surface

2. This friction force will bend the cantilever attached to the AFM tip and change the deflection angle of the laser

3. The photodiode will register a signal that is linearly related to the friction force between sample and tip

Non reciprocal lens on flat



Universal signature of thin films

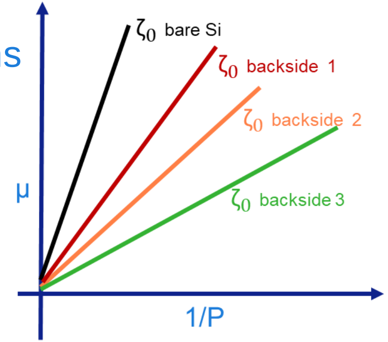
1) $\zeta = \zeta_0 + \alpha P$

Friction force

2) $Ff = A * \zeta_0 + \alpha F_N$

Coefficient of friction

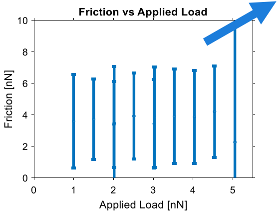
3) $\mu = \frac{1}{P} * \zeta_0 + \alpha$

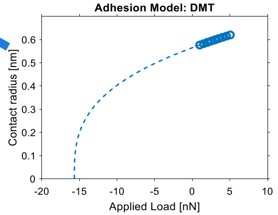


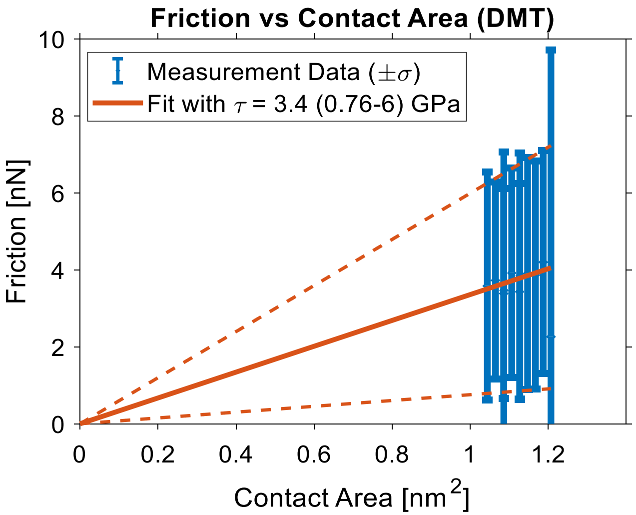
Multiscale approach to assess shear strength

LFM

$$F_f = \tau \times A_{real}$$

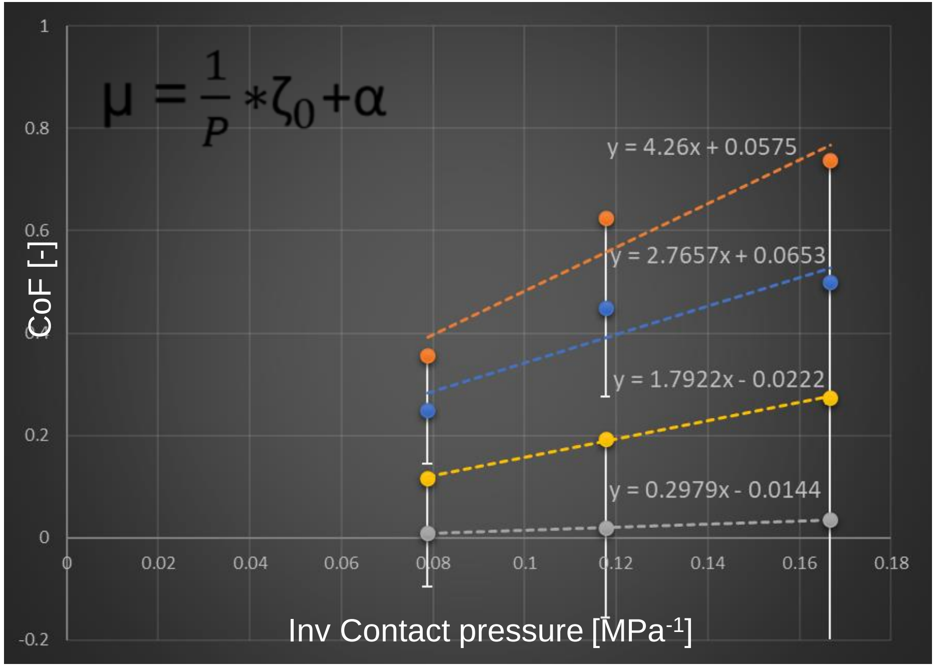






Nanoscale shear strength evaluation of wafer material Vs wafer table material

Non reciprocal lens on flat



Strong influence of roughness and contact “quality” in evaluation shear strength for wafer backside Vs wafer table materials

Summary of our main challenges

1. Nanowear and materials

Real challenge: 5 nm, 10 nm of wear over 1 million wafer passes is already huge ! Any ideal material for low friction (at nm sliding range) and low wear (millions of wafer passes)?

2. Correlation between friction and overlay

Is the shear strength approach quantitatively realistic to capture fundamentals ?

3. Modeling

What is the influence of adhesion, capillary forces, tribocharging at wafer Vs wafer table interface ?

4. Accelerated Lifetime testing (ALT)

How to perform offline ALT testing to predict accurately enough, lifetime of new design choices we made

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